

Atty.
Dkt. No.

M#

Client Ref.

JC08 Rec'd PCT/PTO

25 APR 2001

278095

7048P-U

Applicant: INAGAKI, Yasushi et al

Appln. No.: 09 830,360

Filing Date: April 25, 2001

Examiner:

Group Art Unit: 2827

**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**

Date: April 25, 2001

Page

1

of

1

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR					
	BR					
	CR					
	DR					
	ER					
	FR					

FOREIGN PATENT DOCUMENTS

	Document Number	Date MM/YYYY	Country	Inventor Name	English Abstract	Translation Readily Available
					Enclosed	No
	GR					
	HR					
	IR					
	JR					
	KR					
	LR					
	MR					
	NR					
	OR					
	PR					

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

Q	QR	PATENT ABSTRACTS OF JAPAN, "MULTILAYERED WIRING BOARD" JP 11-126978, May 11, 1999, Akiya.Fujisaki et al
	RR	PATENT ABSTRACTS OF JAPAN "METHOD FOR MANUFACTURING MULTILAYER PRINTED WIRING BOARD", JP 10-013024, January 1, 1998, Satoshi Nakamura
	SR	PATENT ABSTRACTS OF JAPAN, "ELECTRODE STRUCTURE AND THE MANUFACTURING METHOD", JP 54-157296, December 12, 1979
D	TR	PATENT ABSTRACTS OF JAPAN, "MULTILAYER ELECTRONIC PART AND MANUFACTURE THEREOF", JP 8-241827, September 17, 1996
	UR	
	VR	

Examiner JUAN DINW

Date Considered: 12/27/02

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.